A Programmable Gain Amplifier for Automated Gain Control
in Auditory Prostheses

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Abstract

A cochlear implant (CI), also called a bionic ear or electronic cochlea, is an implantable electronic device that can partially restore hearing to profoundly deaf patients by directly stimulating the patient’s auditory nerve via surgically implanted electrode arrays. Hearing impairment of the severely deaf patients translates into a 70-80 dB hearing loss, reaching a hearing dynamic range as low as 15-25 dB. As such, gain control systems are needed in CIs to map the acoustic input signal into the patient’s hearing dynamic range. This paper proposes a programmable gain amplifier (PGA) which can be used to implement a dual-loop automated gain control (AGC). An analog signal processing technique is used, due to its advantages over the digital processing equivalents, such as potentially lower power consumption and higher processing speed. Programming the analog processing parameters, i.e. gain levels and time constants, is done by means of digital control words that set the values of corresponding bias currents. Computation of the control words is done in a digital fashion, allowing a hardware description language implementation of the gain control algorithm. This adds flexibility to the resulting gain control system: ability to choose between a feed-forward and feed-back topology, ability to choose between different compression functions: linear, logarithmic and power-law, and ability to set the desired compression limits. Finally, a fully adaptive gain control system is implemented. The programmable aspect of the adaptive AGC implementation also enables the adjustment of the AGC operation to meet the patient’s individual needs. Circuit simulation proves the functionality of the proposed PGA for automated gain control in CI applications.

Keywords: Cochlear implants, Continuous interleaved sampling, Programmability, Automated gain control

1. Introduction

Cochlear implants (CI), also called bionic ears or electronic cochleae, are implantable electronic devices that can partially restore hearing to profoundly deaf patients by directly stimulating the patient’s auditory nerve via surgically implanted electrode arrays [1]. CIs consist of the following modules: microphone, speech processor, transmitter + receiver system and an electrode array. Their operation consists in receiving, processing and transmitting acoustic signals, leading to direct electrical stimulation of the cochlea. An important feature of recent CIs is the programmable aspect of the speech processor [2] in order to meet the auditory demands of each individual patient.

Recent trends in CI development try to have the sound processor fully implanted, along with the receiver and the electrode array [2]. In such cases, reprogramming of the CI becomes an issue, as the only access to the speech processor is over a wireless link [3]. Thus, programmable analog blocks become of interest for fully implantable speech processors.

A classification of CIs can be done considering the speech processing strategies. A detailed description of the strategies together with their performance is given in [4]. The current research was carried out for a continuous interleaved sampling (CIS) processing algorithm, developed by the Research Triangle Institute (RTI) [www.rti.org]. A description of the algorithm is as follows [1,4]. The speech signal is first compressed/pre-emphasized programmable gain amplifier (PGA) to match the patient’s hearing dynamic range. It is then split into a number of sub-bands by a bank of band-pass filters (BPF). Each sub-band is responsible for the stimulation of a specific area inside the cochlea. The envelopes of the filtered signals are extracted and used to control the amplitude of the stimulation pulses. Finally, trains of non-simultaneous biphasic pulses are generated.

The CIS approach exhibits several programmable parameters for performance optimization [5]: compression function, filter spacing, pulse rate, pulse duration and stimulation order.
This paper proposes a programmable gain amplifier used for gain control, i.e. compression/pre-emphasis, in CIS implants. In respect to gain control, reprogramming of the CI refers to setting the electrical stimulation limits necessary for the CI user to comfortably perceive both soft and loud sounds. An analog signal processing technique has been implemented due to the advantages over its digital equivalent: low power consumption, speed, etc. Parameter control of the analog processing blocks is done in a digital fashion. The targeted application, however, gives a series of constraints to the analog circuitry: low supply voltages, low power consumption, a minimum of 60 dB dynamic range (DR) and the need for high linearity.

The work is organized as follows. First, the issue of gain control in CIs is discussed. Further on, the implementation of a PGA is presented. The proposed PGA will then be used to implement an automated gain control (AGC) system. The functionality of the proposed architectures will be demonstrated by simulation results.

2. Gain control in cochlear implants

Gain control systems in CIs operate such as to meet the needs of severely hearing impaired patients. A healthy ear produces hearing sensations to over 120 dB signal pressure level (SPL) [6]. Hearing impairment translates to a reduction of the acoustical DR by 70-80 dB, which may decrease even further as the frequency increases.

Electrical DR of a CI, which in severely deaf patients is limited to 10–25 dB [6] of electrical signal, must map the entire 120-dB acoustic DR. Therefore, acoustic signal needs to be compressed into the electrical DR suitable for electronic cochlear stimulation. Compression in this case means that loud sounds are attenuated while soft sounds are amplified.

The input stage of a CI is made up by a CI microphone, e.g. Knowles FG-3329A [7] and a preamplifier circuit, e.g. the one described in [8], which provides 20-dB V-V amplification to the microphone signal. In this case, the CIS processor input signal ranges from 50 μV to 530 mV of amplitude, which, in terms of signal pressure levels translates to 30 dB SPL to 110 dB SPL, i.e. 80 dB of input DR.

Adaptive gain control algorithms are employed to permit patients to comfortably perceive soft to loud sounds. The CI input signal needs to be compressed to an instantaneous dynamic range (IDR) of 40-60 dB. For example, the compression of the 50 μV → 530 mV signal to a 60 dB dynamic range results in a 200 μV → 200 mV signal range. The compression ratio (CR) is defined as the ratio of input dynamic range DRIN to the output dynamic range DROUT in dB units, as stated in Eq. (1) [9]:

\[
CR = \frac{DR_{in} (dB)}{DR_{out} (dB)}
\]

For a compression of the input DR, i.e. CR>1, soft sounds are amplified, while loud sounds are attenuated. The gain factor depends on the patient’s hearing profile.

Gain control is done according to a desired input-output function in order to comply with the patient’s hearing needs. Linear compression functions are defined by Eq. (2) [10].

\[
y = Ax + B
\]

where \(x\) [mV] is the acoustic amplitude of the input signal and \(y\) [mV] is the compressed output signal. Further on, logarithmic compression functions are defined by Eq. (3) [11]:

\[
y = A \log(1 + C \cdot x) + B
\]

and power law functions are defined by Eq. (4) [11]:

\[
y = Ax^p + B
\]

Constants A, B and C give the shape of the compression function, and in Eq. (4), \(p < 1\).

3. The programmable gain amplifier

The proposed implementation of a programmable gain amplifier consists of a variable gain amplification (VGA) structure that has its gain set by a digital control word and is presented as follows.

3.1 The VGA

The VGA consists of two wide-linear-range transconductors (WLR) configured in a transconductance-resistance topology [9], as shown in Fig. 1.

![Figure 1. The variable gain amplifier.](image)

The first transconductor, \(G_{m1}\), operates as a voltage-to-current (V-I) converter and is biased by a current \(i_{\text{GAIN}}\). A second transconductor, \(G_{m2}\), with negative feedback, implementing an active resistance, is used as a load for the amplifier and is biased by a current \(i_{\text{REF}}\). The VGA gain is written as:

\[
A_V = \frac{G_{m1} \cdot R_L}{1 + G_{m2} \cdot R_L}
\]

The WLRs from Fig. 1 are implemented with the single-ended Symmetrical Operational Transconductance Amplifier (OTA) topology [12], as shown in Fig. 2, and have been designed to obey the operation conditions in CI applications [13]. For the current design, the factor B will take the value B = 2.
The OTA current gain is given by [12]:

\[
G_m = \frac{i_{out}}{v_{out}} = g_m \cdot B = \frac{2 \cdot i_{bias}}{V_{sat}} \cdot B
\]  
\[
G_m = 1 + G_m \cdot R
\]

where \( g_m \) and \( V_{sat} \) are, respectively, the transconductance and the overdrive voltage of the input transistors, \( B \) is the gain factor of the current mirrors MN1-MN3 and MN2-MN4, and \( i_{bias} \) is the bias current of the input differential stage. Resistive source degeneration has been applied as a linearization procedure. As such, the linearized OTA gain translates to

\[
G_{a,w} = G_m \cdot \frac{1}{1 + G_m \cdot R}
\]

where \( R \) is the degeneration resistance.

As shown in Eq. (7), the circuit is linearized provided that \( R \) is large enough to dominate \( 1/G_m \). In this case, \( 1/G_m \) is negligible compared to \( R \) and thus the OTA gain, \( G_{lin, \text{in}} \), is independent of \( G_m \). For small values of \( R \), however, circuit linearity is limited since \( R \) does not dominate \( 1/G_m \). As such, the OTA gain is dependent on both \( R \) and \( G_m \) and consequently on \( i_{bias} \), according to Eq. (6).

3.2 VGA Gain Control

As expressed in Eq. (5), the VGA gain depends on both \( G_{\text{in}} \) and \( G_{\text{ref}} \). However, it is desirable to keep a constant equivalent resistance value, and consequently a constant bandwidth, while the gain is varied [9].

To be noted, however, is the fact that the OTA gain depends on both OTA bias current and linearization resistance, as shown in Eqs. (6) and (7). Equation (6) shows that the V-I gain, that is \( G_{\text{in}} \), is proportional to \( i_{\text{GAIN}} \). Similarly, \( G_{\text{ref}} \) is proportional to \( i_{\text{REF}} \) and consequently, the equivalent load resistance value is proportional to \( 1/i_{\text{REF}} \). Thus, VGA gain programming can be done by changing the \( i_{\text{GAIN}}/i_{\text{REF}} \) ratio. For example, when \( i_{\text{GAIN}} < i_{\text{REF}} \), the VGA operates as an attenuator. On the other hand, Eq. (7) shows that the V-I gain is dependent on \( 1/R_{\text{GAIN}} \), while the equivalent load resistance is dependent on \( R_{\text{REF}} \), where \( R_{\text{GAIN}} \) and \( R_{\text{REF}} \) denote the source degeneration resistances of the OTAs implementing the V-I converter and the active resistance, respectively. Thus, VGA gain programming can also be done by changing the \( R_{\text{REF}}/R_{\text{GAIN}} \) ratio. Yet, for a constant equivalent resistance, \( i_{\text{REF}} \) and \( R_{\text{REF}} \) will be kept fixed.

Out of practical considerations, variation of \( R_{\text{GAIN}} \) can only be done with a much lower resolution than variation of \( i_{\text{GAIN}} \). In the present design, the \( R_{\text{GAIN}} \) variation step size is 10 kΩ to reach a maximum 71 kΩ, while the \( i_{\text{GAIN}} \) variation step size is 2.5 μA to reach a maximum 80 μA. According to Eq. (7), gain variation will be much stronger at one step change in \( R_{\text{GAIN}} \) than in \( i_{\text{GAIN}} \). The exact gain variation step size is, however, dependent on the value of either \( R_{\text{GAIN}} \) or \( i_{\text{GAIN}} \), whichever is kept fixed.

It is thus sensible to consider \( R_{\text{GAIN}} \) for hard tuning and \( i_{\text{GAIN}} \) for fine-tuning of the VGA gain. The VGA gain is controlled as shown in Table 1. High VGA gains are achieved with small degeneration resistance and high bias current values. Lower VGA gains are achieved for higher degeneration resistance and lower bias current values. Moreover, digital control of these two parameters gives a digital control of the VGA gain.

**Table 1. Variation of the VGA gain in respect to the OTA degeneration resistance \( R_{\text{GAIN}} \) and the bias current \( i_{\text{GAIN}} \).**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VGA Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>Degeneration ( R )</td>
<td>( G_{\text{in}} ) ↓</td>
</tr>
<tr>
<td>( i_{\text{GAIN}} )</td>
<td>( G_{\text{in}} ) ↓</td>
</tr>
</tbody>
</table>

Digital control of the degeneration resistance is done directly by means of the switched series resistor array implemented for source degeneration, as shown in Fig. 2. The OTA linearization resistance is then implemented with a number of resistors in a series connection. Three PMOS switches control the actual value of the degeneration resistance, allowing 8 resistance values, that is, 8 different VGA gains.

Digital control of the V-I converter bias current is achieved by having \( i_{\text{GAIN}} \) sourced with a current division network (CDN). A detailed description of the CDN and its employment is given in the next section.

3.3 Current division network

A CDN is a cascade of \( n \) current division cells (CDC), as shown in Fig. 3 [14]. Each CDC divides its input current and feeds it to the output branch of the division network. A copy of the divided current is also fed to the next CDC for further division. The output current of the CDN is given by [14]:

![Figure 2. The symmetrical WLR OTA with resistive source degeneration.](image-url)

![Figure 3. (a) CDN block diagram. (b) CDN symbol.](image-url)
and is a weighted sum of input current fractions. As shown, the control bit \(a_i\) decides whether a current fraction is added to the output current or not. Thus, the CDN output current is controlled by a digital word \(a = [a_0, \ldots, a_i, a_7]\). To be noted is that one instance of the CDN output current is unconditionally added to the CDN output sum.

The implementation of a CDC is shown in Fig. 4 where a differential stage is used as the current division element. Using this implementation, the limitations of MOS divider structures, such as transistor matching and CDN length limitation, are avoided [14]. Cascading was also employed to increase the output resistance and, consequently, the precision of the current division.

![Figure 4. CDC circuit schematic.](image)

To source the bias current \(i_{\text{GAIN}}\) needed for the present application, a five-cell CDN (CDN5) will be needed, with its input current set to 80 \(\mu\)A. This gives a 2.5-\(\mu\)A resolution for current adjustment within the range of 2.5 \(\mu\)A to 80 \(\mu\)A.

The proposed implementation of the PGA and its equivalent symbol are shown in Fig. 5. The solution proposed in this article for having a digital control of the PGA gain is as follows: the V-I converter degeneration resistance is controlled by three bits, \([a_5, a_3, a_1]\), and its bias current \(i_{\text{GAIN}}\) sourced by means of a CDN5 with 5 control bits, \([a_5, a_4, a_3, a_2, a_1]\). As such, the PGA is controlled by an 8-bit digital word: \(a = [a_5, a_4, a_3, a_2, a_1, a_1, a_0, a_0]\).

### 4. Automated gain control

The role of the PGA in the CIS CI is to compress the speech signal into a targeted DR, following a desired compression function. If gain adaptation is done by sensing the speech signal levels, i.e. the envelope of the speech signal, the PGA will actually implement an AGC. A classification can be done as follows [9]. If gain adaptation is done using the PGA input signal, it is the case of a feed-forward AGC. If the output signal is used, it is the case of a feed-back AGC.

Signal level, i.e. envelope sensing, is done by means of an envelope detector structure, which sets the AGC temporal dynamics [9]: the attack time constant for soft-to-loud transitions, and the release time constant for loud-to-soft transitions. The time constants set the time needed for the AGC to adapt to changes in sound intensity. Yet, another distinction can be made as follows [9]. If the AGC has one set of time constants, it is the case of a single-loop AGC. If the AGC has two sets of time constants, it is the case of a dual-loop AGC.

All-analog AGC implementations are presented in [9]. In those cases, gain control is done within a translinear loop that implements the desired compression function: linear, logarithmic or power-law. It is shown [9] that feed-forward controllers are more difficult to implement, but exhibit better circuit performance. Feed-back controllers on the other hand are easier to implement, but suffer from instability. It is also shown [9] that for an analog dual-loop AGC, several additional circuits are needed, e.g. a current comparator and a hold timer, which add to the system complexity.

Digital gain control will, however, overcome the limitations of all-analog gain control circuits presented in [9]. Gain control is done in a digital computation structure, and algorithms can be implemented in hardware description code, e.g. VHDL. As such, it is easy to implement both feed-forward and feed-back control functions. Stability restrictions can also be easily set. Furthermore, dual-loop AGC algorithms don’t require additional circuitry as comparison and timing are also done in a digital manner.
The block diagram of the proposed dual-loop AGC is shown in Fig. 6. As can be seen, a PGA was used as the amplification element. The translinear controller from the all-analog AGC implementation [9] is replaced by a digital computation structure. A set of MOS switches allows choice of either a feed-forward or feed-back AGC topology.

In the AGC in Fig. 6 envelope detection is done by a structure made up of a current rectifier and a peak detector. Their implementation is described in [13] and is based on [15]. The attack and release time constants of the peak detectors are controlled by corresponding bias currents. The digital control of the AGC temporal dynamics is achieved by sourcing the envelope detector (ED) bias currents with CDNs. As such, the AGC time constants are set by means of a digital control word. Finally, the A-D conversion is done using the algorithmic ADC implemented with current mirrors [16].

A description of the dual-loop gain control algorithm [9] is given as follows and is based on the Moore algorithm. The block diagram of the dual-loop gain control algorithm is then shown in Fig. 7. For gain control, the Moore algorithm uses two signal envelopes provided by the two EDs from Fig. 6. One ED implements slow time constants, while the other implements fast time constants for tracking the abrupt changes in signal level. Which of the two signal envelopes determines the AGC gain is conditioned by the state of a hold-timer as follows: if the hold-timer state is charged, i.e. logical ‘1’, the fast envelope gives the AGC gain and the slow ED is used for signal tracking; if the hold-timer state is discharged, i.e. logical ‘0’, the slow envelope gives the AGC gain and the slow ED holds its state. The state of the hold-timer is determined by the larger of the two envelopes, considering a set of delay times and a 0.4 attenuation of the fast envelope.

5. Results

The proposed circuits have been implemented and simulated with Eldo from Mentor Graphics [www.mentor.com]. The simulations were performed for differential Vdd = -Vss = 1.5 V supply voltages.

First, the voltage transfer characteristic (VTC) of the PGA in Fig. 5 is presented. The bias current of the active resistance, \( I_{REF} \), was kept fixed at 20 \( \mu A \) and its source degeneration resistance \( R_{REF} \) at 10 k\( \Omega \). As such, the VTC was deduced by variation of the V-I converter parameters: \( I_{GAIN} \) and \( R_{GAIN} \). Figure 8 shows the VTC of the PGA when \( I_{GAIN} \) was set to 20 \( \mu A \) and \( R_{REF} \) varied from 1 k\( \Omega \) to 61 k\( \Omega \) with a step size of 10 k\( \Omega \). In this case, the PGA voltage gain varied from 1.13@\( R_{GAIN} = 1 \) k\( \Omega \) to 0.3@\( R_{GAIN} = 61 \) k\( \Omega \). Figure 9 shows the VTC of the PGA when \( R_{GAIN} \) was set to 11 k\( \Omega \) and \( I_{GAIN} \) varied from 0.91–4.07. Table 2. The available gain ranges for different values of the source degeneration resistance \( R_{GAIN} \).

![Figure 6. AGC block diagram.](image)

![Figure 7. Block diagram of the dual loop gain control algorithm.](image)

![Figure 8. PGA DC transfer characteristic for variable \( R_{GAIN} \) with \( I_{GAIN} = 20 \mu A \).](image)

<table>
<thead>
<tr>
<th>( R_{GAIN} (k\Omega) )</th>
<th>1</th>
<th>11</th>
<th>21</th>
<th>31</th>
<th>41</th>
<th>51</th>
</tr>
</thead>
<tbody>
<tr>
<td>PGA gain</td>
<td>0.91–4 0.76–4</td>
<td>0.80–5.59–1.26</td>
<td>0.5–1.15</td>
<td>0.43–1</td>
<td>0.38–1</td>
<td></td>
</tr>
</tbody>
</table>

The block diagram of the proposed dual-loop AGC is shown in Fig. 6. As can be seen, a PGA was used as the amplification element. The translinear controller from the all-analog AGC implementation [9] is replaced by a digital computation structure. A set of MOS switches allows choice of either a feed-forward or feed-back AGC topology.
was varied from 10 μA to 80 μA with a step size of 10 μA. In this case, the PGA voltage gain varied from 0.76@_{i_{\text{GAIN}}} = 10 μA to 1.48@_{i_{\text{GAIN}}} = 80 μA. Considering a sweep of \( i_{\text{GAIN}} \) from 10 μA to 80 μA, the PGA gain variation range for different \( R_{\text{GAIN}} \) values is given in Table 2.

![PGA DC transfer characteristic for variable \( i_{\text{GAIN}} \) with \( R_{\text{GAIN}} = 11 \text{kΩ} \)](image)

The VTCs in Figs. 8 and 9 prove the linear range of the VGA upon the range of interest. Indeed, for small values of \( R_{\text{GAIN}} \), the linear range is limited to ± 150 mV which however covers the input signal range that needs high amplification, i.e. \( V_{\text{IN}} < 150 \text{mV} \). Similarly, for small values of \( i_{\text{GAIN}} \), linearity is limited again. Yet, considering the PGA programmability by means of \( R_{\text{GAIN}} \) and \( i_{\text{GAIN}} \), an adequate combination of the two parameters leads to linearity over the targeted input signal range. The adequate \( R_{\text{GAIN}} + i_{\text{GAIN}} \) combinations for different input signal levels, which give the targeted gain value and linear range, are listed in Tables 3, 4 and 5.

Based on the PGA simulation results, the total harmonic distortion (THD) was computed to be 0.35%, with a maximum level of 1.09% for the highest compression factor (PGA gain = 0.37). The power consumption of the VGA was computed to a mean value of 354 μW, reaching 786 μW for the highest achievable gain, i.e. 4 (linear) @\( R_{\text{GAIN}} = 1 \text{kΩ} \) & \( i_{\text{GAIN}} = 80 \mu A \).

For demonstration of the full gain control circuit for an 80 dB → 60 dB DR compression, CR = 1.33, the feed-forward topology of the AGC from Fig. 6 was simulated. The peak detectors were programmed to implement the time constants listed in Table 6, which result from medical studies [17]. The parameters \( i_{\text{GAIN}} \) and \( R_{\text{GAIN}} \) for a desired amplification are computed within the Gain Control block from Fig. 7 as follows. \( R_{\text{GAIN}} \) is determined from a look-up-table (LUT) similar to Table 2 such that the amplification range covers the targeted gain value. Considering that the gain range for different \( R_{\text{GAIN}} \) values overlap (see the different columns in Table 2), the appropriate value is chosen such as to meet the OTA linearity condition, roughly expressed as function.

\[
g_+ > > \frac{1}{R} \tag{9}
\]

For the chosen \( R_{\text{GAIN}} \), \( i_{\text{GAIN}} \) is varied such as to increase or decrease the amplification in order to meet the desired compression characteristic.

### Table 3. Parameters of the AGC simulation with linear compression.

<table>
<thead>
<tr>
<th>( V_{\text{IN}} ) (mV)</th>
<th>( V_{\text{OUT}} ) (expected)</th>
<th>Gain</th>
<th>( R_{\text{GAIN}} ) (kΩ)</th>
<th>( i_{\text{GAIN}} ) (μA)</th>
<th>( V_{\text{OUT}} ) (simulated) (mV)</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>530</td>
<td>200</td>
<td>0.37</td>
<td>51</td>
<td>12</td>
<td>205</td>
<td>2.5%</td>
</tr>
<tr>
<td>300</td>
<td>114.2</td>
<td>0.38</td>
<td>51</td>
<td>10</td>
<td>118</td>
<td>3.3%</td>
</tr>
<tr>
<td>200</td>
<td>76.2</td>
<td>0.38</td>
<td>51</td>
<td>8</td>
<td>75</td>
<td>1.5%</td>
</tr>
<tr>
<td>100</td>
<td>38.2</td>
<td>0.38</td>
<td>51</td>
<td>8</td>
<td>39</td>
<td>2%</td>
</tr>
<tr>
<td>50</td>
<td>19.2</td>
<td>0.38</td>
<td>51</td>
<td>10</td>
<td>18.5</td>
<td>3.6%</td>
</tr>
<tr>
<td>500</td>
<td>238</td>
<td>2.38</td>
<td>41</td>
<td>28</td>
<td>244</td>
<td>2.5%</td>
</tr>
<tr>
<td>50</td>
<td>200</td>
<td>4</td>
<td>1</td>
<td>80</td>
<td>210</td>
<td>5%</td>
</tr>
</tbody>
</table>

### Table 4. Parameters of the AGC simulation with logarithmic compression.

<table>
<thead>
<tr>
<th>( V_{\text{IN}} ) (mV)</th>
<th>( V_{\text{OUT}} ) (expected)</th>
<th>Gain</th>
<th>( R_{\text{GAIN}} ) (kΩ)</th>
<th>( i_{\text{GAIN}} ) (μA)</th>
<th>( V_{\text{OUT}} ) (simulated) (mV)</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>530</td>
<td>200</td>
<td>0.37</td>
<td>51</td>
<td>12</td>
<td>205</td>
<td>2.5%</td>
</tr>
<tr>
<td>300</td>
<td>181.8</td>
<td>0.6</td>
<td>31</td>
<td>20</td>
<td>183</td>
<td>0.66%</td>
</tr>
<tr>
<td>200</td>
<td>168.8</td>
<td>0.84</td>
<td>21</td>
<td>36</td>
<td>165</td>
<td>2.25%</td>
</tr>
<tr>
<td>100</td>
<td>146.7</td>
<td>1.47</td>
<td>11</td>
<td>70</td>
<td>148</td>
<td>0.88%</td>
</tr>
<tr>
<td>50</td>
<td>124.8</td>
<td>2.5</td>
<td>1</td>
<td>80</td>
<td>126</td>
<td>1.6%</td>
</tr>
<tr>
<td>50</td>
<td>200</td>
<td>4</td>
<td>1</td>
<td>80</td>
<td>210</td>
<td>5%</td>
</tr>
</tbody>
</table>

### Table 5. Parameters of the AGC simulation with power-law compression.

<table>
<thead>
<tr>
<th>( V_{\text{IN}} ) (mV)</th>
<th>( V_{\text{OUT}} ) (expected)</th>
<th>( G_{\text{IN}} )</th>
<th>( R_{\text{GAIN}} ) (kΩ)</th>
<th>( i_{\text{GAIN}} ) (μA)</th>
<th>( V_{\text{OUT}} ) (simulated) (mV)</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>350</td>
<td>200</td>
<td>0.37</td>
<td>51</td>
<td>12</td>
<td>205</td>
<td>2.5%</td>
</tr>
<tr>
<td>300</td>
<td>174.9</td>
<td>0.58</td>
<td>31</td>
<td>16</td>
<td>176</td>
<td>0.62%</td>
</tr>
<tr>
<td>200</td>
<td>158.5</td>
<td>0.79</td>
<td>21</td>
<td>30</td>
<td>160</td>
<td>0.94%</td>
</tr>
<tr>
<td>100</td>
<td>133.3</td>
<td>1.33</td>
<td>11</td>
<td>58</td>
<td>136</td>
<td>2%</td>
</tr>
<tr>
<td>50</td>
<td>111.3</td>
<td>2.23</td>
<td>1</td>
<td>70</td>
<td>116</td>
<td>4.2%</td>
</tr>
<tr>
<td>50</td>
<td>200</td>
<td>4</td>
<td>1</td>
<td>80</td>
<td>210</td>
<td>5%</td>
</tr>
</tbody>
</table>
Table 6. AGC temporal dynamics.

<table>
<thead>
<tr>
<th>Detector Type</th>
<th>Attack Time Constant $\tau_a$</th>
<th>Release Time Constant $\tau_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast envelope detector</td>
<td>2–4 ms</td>
<td>70–80 ms</td>
</tr>
<tr>
<td>Slow envelope detector</td>
<td>240–300 ms</td>
<td>1–1.5 s</td>
</tr>
</tbody>
</table>

First, the gain control algorithm was implemented with the linear compression function expressed in Eq. (2), with $A = 0.38$ and $B = 0.2$. For different input voltage amplitudes ($V_{IN}$), the expected output voltage ($V_{OUT}$), the PGA gain (Gain), the simulated output voltage ($V_{OUT}$) and the resulting error are listed in Table 4. The VTC of the AGC with linear compression function is plotted in Fig. 10 for both cases: ideal and simulated.

Second, the gain control algorithm implements the logarithmic function from Eq. (3), with $A = 73.9$, $B = -1.38$ and $C = 1$. The simulation results are listed in Table 5. The VTC of the AGC with logarithmic compression function is plotted in Fig. 11.

Third, the gain control algorithm implements the power-law function from Eq. (4), with $A = 67.5$, $B = -36.25$ and $p = 0.2$. The simulation results are listed in Table 6. The VTC of the AGC with power-law compression function is plotted in Fig. 12.

The simulation results demonstrate the functionality of the proposed PGA structure for gain control applications. A maximum voltage gain that can be achieved with this structure is however limited to $4@R_{GAIN} = 1$ kΩ and $i_{GAIN} = 80$ $\mu$A.

Finally, a comparison between the AGC proposed in this article and solutions previously proposed is given in Table 7. It should be noted that little literature is available on the topic of gain control in CIs. The works reported in [19] and [20], for example, provide an AGC solution for hearing aid devices, thus following slightly different specifications. As it is shown in Table 7, the proposed AGC boasts with the aspect of full programmability via CDN, which translates to an increased flexibility in the implementation of the gain control loop: feed-forward/feed-back, linear/logarithmic/power-law compression, gain control algorithm (by means of HDL), etc. The power consumption is, however, high compared to previous solutions, a problem which will be treated in further development activities.

![Figure 10. AGC transfer characteristic for a linear compression function.](image1)

![Figure 11. Logarithmic compression function.](image2)

![Figure 12. Power-law compression.](image3)

<table>
<thead>
<tr>
<th>Table 7. Comparison of the proposed AGC with previous solutions.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Functionality</td>
</tr>
<tr>
<td>----------------</td>
</tr>
<tr>
<td>This work AGC</td>
</tr>
<tr>
<td>[9] Single/Dual-loop AGC</td>
</tr>
<tr>
<td>[18] Single-loop</td>
</tr>
<tr>
<td>[19] Single-loop</td>
</tr>
<tr>
<td>[20] Single-loop</td>
</tr>
</tbody>
</table>
6. Conclusions

This paper has presented the CMOS implementation of a PGA used for AGC in CI applications. An implementation of a digital gain control method was proposed, allowing for increased flexibility in the choice and implementation of the compression function and the mapping limits. The simulation results show the functionality of digital control in setting the gain of the analog amplification block.

The limitations of the proposed amplifier regard the high amplification of low signal levels which is needed for the implementation of the non-linear compression functions. To handle these limitations, the AGC structure requires an alternative amplification approach, which implies parallel amplification routes to cover different amplification range requirements. A solution to this problem requires further research.

Acknowledgements

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References