Integrated System for Improving Electrical Safety of Biochips

Robert Rieger*  Chi-Huai Chang

Electrical Engineering Department, National Sun Yat-Sen University, Kaohsiung 804, Taiwan, ROC

Received 18 Jul 2012; Accepted 12 Oct 2012; doi: 10.5405/jmbe.1233

Abstract

A safe electrical connection between an integrated circuit and the human body is required for the recording of physiological signals such as electrocardiogram, electronystagmogram, and electromyogram signals. The recording chip is typically connected to the patient through a blocking capacitor, which prevents the flow of direct current in the event of circuit failure. However, in systems with a high integration density, blocking capacitors are inconvenient due to their large size and their effect on the signal transfer function. Therefore, this study proposes a fully integratable functional monitoring scheme which involves applying a test signal to the amplifier input and detecting its presence at the output. In the event of failure, the resulting change in the output voltage is detected and the chip can be switched into a safe state. Test signal addition and extraction circuits are proposed and analyzed. Measurement results are presented to confirm the correct operation in the context of a typical recording front-end.

Keywords: Implantable or wearable circuit, Biopotential recording, Electrical patient safety, Integrated circuit design

1. Introduction

With recent advances in technology, the full integration of signal acquisition systems for physiological signals on a single chip has become feasible. Typical applications include the recording of the electrical signals associated with heart, peripheral nerve, or muscle activity including electrocardiogram (ECG), electronystagmogram (ENG), and electromyogram (EMG) signals, respectively [1-5]. The signals at the recorder input obtained with typical electrodes are small, on the order of microvolts (natural ENG) to millivolts (EMG, ECG). High-gain amplifiers are conventionally connected to the electrodes by alternating current (AC) coupling to reject electrode offset voltages. However, as physiological signals occupy a low-frequency band, the cut-off frequency of the input filter must also be very low. For example, the recording of ECG requires a cut-off frequency of less than 0.5 Hz [6]. In principle, direct current (DC)-coupled systems can be used to overcome this design challenge even in the presence of offset and interference [7,8]. However, DC coupling is limited by safety concerns, as the flow of current in the input leads must be kept at a safe level even in the event of circuit failure. Lacking a series input capacitor, failure currents can potentially flow directly into the patient.

The limit of the tolerable failure current depends on a number of factors, including the signal frequency and the contact area [9]. The catheter current should be limited to a maximum of around 10 µA to prevent a microshock and resulting fibrillation of the heart [6,9]. For implanted devices which interface directly with the peripheral nervous system or with muscle fibers [10-12], the charge flux must be limited to prevent electrode and tissue damage as well as inadvertent stimulation. Prolonged direct current flow is not permissible even at relatively low current levels due to the ensuing electro-chemical effects at the electrode-tissue interface, which can lead to electrode and tissue damage. Charge-balanced current waveforms (i.e., AC signals), however, may safely reach higher peak amplitudes. For implanted stimulation devices of muscle, a charge density of 0.4 µC/mm² of electrode area delivered in 50 Hz intervals was established as a safe limit [13]. A study of nerve stimulators [14] found that charge-balanced signals do not cause significant tissue damage at levels of up to 2 µC/mm² per pulse. Thus, assuming a typical electrode area of 2.5 mm² [15], the maximum permissible electrode charge is around 1 µC. Presuming a sinusoidal waveform, the equivalent peak current amplitude \( I_p \) is calculated as:

\[
Q = \frac{1}{\pi} \int I_p \sin(2\pi f t) dt \rightarrow I_p = Q \cdot \pi \cdot f
\]

(1)

where \( Q \) is the charge and \( f \) is the signal frequency. From Eq. (1), failure current is practically limited by the 10 µA level to prevent fibrillation. Considerably higher currents are needed for functional nerve stimulation as in [12,13,16].

While offset currents can be controlled to within safe levels by careful circuit design, failure currents in the event of device breakdown are difficult to manage. As in a CMOS design, the input leads typically connect to the high-impedance gates of the input devices, and thus failure of the gate oxide is a critical weak point. Gate oxide breakdown in the input devices

* Corresponding author: Robert Rieger
Tel: +886-7-5252000 ext. 4188; Fax: +886-7-5254199
E-mail: rieger@mail.nsysu.edu.tw
can lead to a gate oxide short (GOS) [17], in which a point of the MOS channel connects to the gate, providing a path for failure current. Active detection of a short condition and of the lowering of the gate impedance, which may be considered a pre-cursor to eventual total breakdown, is proposed in this paper. Detecting immanent failure allows initiating an appropriate emergency response, which most simply involves interrupting the power supply to the affected input stage.

Sensing the failure current directly in the patient leads is not feasible, as the sensing circuit may also suffer a failure and cause harmful lead currents. Therefore, indirect detection of the fault condition is proposed via the monitoring of the output voltage of the preamplifier. Catastrophic electrical fault of the input transistors is expected to lead to saturation of the amplifier and latching of the output voltage to either of the supply rails, similar to a stuck-at-fault in a digital circuit (although electrode breakage may also cause this effect). A mere lowering of the gate input impedance or symmetrical faults on both differential input devices may not be detected in this way. Therefore, an on-chip monitoring system is proposed and analyzed in Section 2, which attempts to detect changes in the input transistor characteristics by applying a test signal and monitoring the amplifier output response. This is an improved version of the system the authors described in [18]. Transistor-level simulation results are presented in Section 3. A mismatch analysis, which is essential for designing a robust practical circuit, is also provided. Furthermore, the measurement results obtained from an integrated circuit implementation (ASIC) are presented in Section 4. Conclusions are given in Section 5.

2. Proposed monitoring system

2.1 Test signal application

GOS is characterized by a substantial lowering of the gate impedance, which enables current to flow between the gate terminal of the affected input device and its channel [17]. Consequently, the performance of the input device is affected, which is detectable by observing the amplifier output. Active monitoring using the circuit principle shown in Fig. 1 is proposed. A small, test signal is applied to the input devices.

![Figure 1. Principle diagram of the proposed functional monitoring system.](image)

An amplified signal is measured at the amplifier output during normal operation but it is considerably reduced in magnitude in the event of failure. The test signal frequency is chosen to be higher than the bandwidth of the physiological signal to be recorded. Therefore, the test signal can be added to the physiological signal and amplified together. After amplification, the test signal is separated from the physiological signal using a set of filters. The diminishing of the test signal at the specified frequency can be used to trigger the failure alarm. Since the bandwidth of physiological signals is typically limited to a few kilohertz, the input amplifier can be designed to provide a wider bandwidth with a tolerable increase in power consumption [19]. In fact, the amplifier bandwidth is often much higher than required and is reduced using low-pass filters. Figure 2 shows the principle of adding the test signal to the physiological signal. The test signal is coupled to a small resistor \( R_t \) in the input lead using capacitors, which are small enough to be implemented on-chip. Therefore, a failure in the test signal generator does not lead to a DC failure current in the patient leads. Also, no leakage current can flow and the amplifier input impedance in the physiological bandwidth is not significantly affected. This input arrangement is analyzed using its equivalent differential circuit, shown in Fig. 3. The amplifier input impedance in normal operation is assumed to be large enough to be negligible. The signal appearing across the amplifier terminals, i.e., the gates of the input devices, is \( V_{n} \).

![Figure 2. Principle diagram showing how the test signal is added to the physiological signal using on-chip blocking capacitors to maintain patient safety.](image)

![Figure 3. Equivalent circuit of the input side of Fig. 2 used for analysis.](image)
DC current, allowing only a small AC current $i_t$ to flow in the leads. Analysis of the circuit shows that the test voltages cause an electrode current to flow as follows (here calculated for electrode $Z_{c1}$):

$$i_t = \frac{V_i (Z_{c1} + R'_t) + V_e (Z_{c1} + R_t)}{Z_{c1}(Z_{c1} + R'_t + Z_s) + R_t(Z_{c1} + R'_t + Z_s) + Z_{c1}(Z_{c1} + R'_t)}$$

(2)

where $R_t$ and $R'_t$ and $Z_s$ and $Z'_c$ are respectively designed to have identical nominal values. Letting $R_t = R'_t = R$ and $Z_{c1} = Z_{c2} = Z_c$, simplifies Eq. (2) to:

$$i_t = \frac{2V_{cm}}{R + 2Z_c}$$

(3)

where the undesired common-mode (CM) component of the test voltage $V_{CM}$ is defined as $(V_i + V_e)/2$. This confirms that due to the symmetry of the circuit, in the patient lead as long as matched test signal sources are used ($V_i = V_{CM} = V_e$). Also, the typical electrode impedance $Z_s$ is in the range of a few kilohms so that $Z_c$ is large compared to both $Z_s$ and $R$. Then, $i_t$ scales with $1/Z_c$, approaching negligibly small amplitudes even in the presence of finite $V_{CM}$.

Assuming matched components, the test signal $V_{in}$ appearing at the amplifier input is:

$$V_{in} = (V_i - V_e) \frac{R}{R + Z_c} + V_{cm} \frac{2Z_c (Z_{c1} - Z_{c2})}{(R + Z_c) + 2Z_{c2}}$$

(4)

CM break-through on $V_{in}$ is in proportion to the electrode mismatch $Z_{c1}-Z_{c2}$. Since this mismatch is not controlled by the circuit designer, the CM voltage on the test sources should be kept to a minimum. The effect of mismatch between the resistors and capacitors is examined in Section 3.

$V_{in}$ should be of moderate amplitude to allow reliable detection without limiting the dynamic performance of the system. Therefore, a practical trade-off must be sought for the values of $C$, $R$, and the amplitude and frequency of $V_i$. A test signal frequency of 1 MHz is selected as it is well outside the physiological bandwidth and it can conveniently be generated on-chip using an OTA-C oscillator [20]. $R$ is limited to a few kilohms by circuit area constraints. To generate $V_i$ on an integrated circuit, an amplitude of around 1 Vpp is suitable. The required capacitance thus depends on the targeted amplitude of $V_{in}$. The minimum amplitude for $V_{in}$ depends on the detection accuracy of the test signal at the amplifier output and it is thus dependent on the amplifier characteristics. To obtain an initial estimate of the design parameters, a typical pre-amplifier DC gain of 200 and $R = 1$ kΩ are chosen. Assuming a -3 dB cut-off frequency of 50 kHz for the input stage and a first-order characteristic, the remaining gain at 1 MHz is calculated to be slightly less than 10 V/V. For reliable detection, an output amplitude of at least 40 mVpp is targeted. Using Eq. (4) yields a required impedance of about 1 MΩ at the test signal frequency, implying a capacitance of approximately 160 fF.

2.2 Test signal detection

The detailed implementation of the detection circuitry largely depends on the application area and the affordable complexity. A block diagram and a flowchart for a simple provisional implementation are shown in Fig. 4. The generated test signal is used as a timing reference. Continuous-time comparator $K2$ converts the sinusoidal oscillator signal into a square wave clock compatible with digital logic. It is delayed by $D1$ to trigger edge-clocked inverting comparator $K1$ near the expected peaks of the received signal, thus also converting the received signal into a digital waveform. An exclusive-or connection between the comparator output and the clock signal yields a continuous high level as long as the test signal is received correctly. Double-edge triggered D-type flip-flop $L2$ is used to sample the signal periodically. Upon the disappearance of the test signal, $L2$ begins to produce a square wave output, which increases a 3-bit up-counter. The most significant bit (MSB) of the counter is used to raise the alarm by setting flip-flop $L3$. The counter is reset periodically. Introducing the counter in the detection chain reduces the probability of false alarms due to spurious interference (e.g., temporary saturation of the amplifier), as the absence of the test signal must be detected over several clock cycles before the alarm is triggered. In addition, a practical input stage uses offset and drift removal to reduce the chance of saturation [8,15].

Figure 4. (a) Block diagram of a circuit implementation for the detection of the test signal and for triggering the alarm in the event of failure. This circuit is followed by a 3-bit counter to reduce false alarms caused by interference. (b) Simplified failure detection flowchart and corresponding circuit waveforms for normal operation and GOS (red).

3. Performance evaluation

3.1 Device mismatch evaluation

In any practical implementation, even nominally identical components exhibit mismatch. This mismatch affects the accuracy of the assumptions made in the derivation of Eq. (3) and (4). To characterize the effect of mismatch on the electrode current and input voltage, relation (2) and the corresponding expression for $V_{in}$ are evaluated using Matlab software (The MathWorks, Natick, MA, USA). A large number of simulation runs ($N = 100,000$) are performed to yield a statistical distribution of $i_t$ and $V_{in}$ under the assumption of normally distributed device variation. Each circuit element is varied individually in a Gaussian distribution from its nominal value with standard deviations of 1% for the resistors and 0.1% for
the capacitors, which is representative of the on-chip variation expected in an integrated circuit. Furthermore, the process-dependent inter-die variation is considered. Since the limits of these variations are ultimately controlled by the foundry, a uniform random distribution is chosen and added to the on-chip mismatch variation. All capacitors in this study experience a common variability of ± 10% around their nominal value and resistors vary by ± 20%. The simulations are performed for three magnitudes of electrode impedance $Z_e$, namely 1, 10, and 100 kΩ. In the first set of simulations, the test signal sources are purely differential with $V_{t1} = -V_{t2} = 1 \text{ mV}_{pp}$. The data are shown in the histograms of Fig. 5(a), each comprising 100 sample bins. The distribution plots yield the following observations:

$$V_{t1} = V_{t2} = V_{CM} = 20 \text{ mV}.$$ The histogram showing the electrode current is given in Fig. 5(b). The electrode current spread is dominated by inter-die variation with ± 10% bounds around the mean value of 4 mV. Capacitance variation is the dominating effect, as $i_e \approx 2V_{cm}/Z_e$ (from Eq. (3)). Also, the CM portion of Eq. (4) can be approximated to yield $V_{t} = 2V_{CM}/Z_e \langle Z_e \rangle$. Here, the spread is further affected by a mismatch between the electrode impedances. Care should be taken to minimize the CM component of the test signal sources to avoid interfering with the differential test signal detection.

### 3.2 System simulation

The circuit of Fig. 2 and the detection circuit of Fig. 4 are simulated using the Spectre simulator in the Cadence design environment (Cadence Design Systems, San Jose, CA, USA). The fully differential amplifier provides a first-order roll-off with a cut-off frequency at 158 kHz, a DC gain of 200, and infinite input impedance. Each amplifier output is followed by a passive filter network, as shown in Fig. 6. The filter separates the low-frequency physiological signal $V_{physio}$ for further processing and the test signal $V_{test}$ for continuous monitoring. The transfer gain from the electrode input and from the test signal generator to the filter outputs is plotted in Fig. 7. It is observed that the test signal appears attenuated by over -53 dB at the physiological filter output ($V_{physio}/V_t$) whereas lead input $V_e$ receives a gain of +46 dB ($V_{physio}/V_t$). The test signal is received with an attenuation of -18.8 dB at the test output ($V_{test}/V_t$), as expected from Eq. (4). Since there is no significant continuous physiological activity at 1 MHz, the gain from the amplifier input to the test output ($V_{test}/V_e$) is not expected to affect functionality.

![Figure 5](image1.png)  
**Figure 5.** Histogram of the effects of device mismatch and load resistance $Z_e$ on the differential patient lead current and amplifier input test signal voltage at 1 MHz. (a) Differential and (b) common mode test signals.

![Figure 6](image2.png)  
**Figure 6.** Passive filter used to separate test signal and physiological signal.

![Figure 7](image3.png)  
**Figure 7.** Transfer gain of the system from electrode to filter output and test generator to filter output. Electrode voltage $V_e = V_{test1} - V_{test2}$ in Fig. 2.
Figure 8 shows the simulation results in the time domain. A 1 kHz sinusoidal signal with a 200 μVpp amplitude representing a physiological signal was applied together with a 1 MHz, 1.4 mVpp test signal. The resulting superpositioned $V_{in}$ is plotted in the top trace. The center trace shows the output of the test signal filter. The test signal is successfully extracted, yielding a differential amplitude of around 40 mVpp, as expected. The bottom trace is the output of the physiological signal filter. It is observed that the test signal is removed, leaving the amplified 1 kHz signal available for further processing. The schematic of Fig. 9 is used to simulate the performance of the system for a suddenly occurring defect. An OTA-C oscillator with differential output [20] is implemented and used to generate the test signal input. A differential gain stage with NMOS input devices models the gain stage. The GOS is incorporated by splitting the input devices into two series transistors so that the common gate can be connected to the center point (channel) through a 100 Ω resistor in series with a switch [17]. The detection circuit of Fig. 4 is also included in the simulation. In normal operation, the GOS switch is open and the test signal is received at the filter output. After 10 μs, the switch is closed to simulate a GOS, causing a 5 μA failure current to flow from the amplifier into the affected input lead. As required, the test signal immediately disappears, as shown in Fig. 10. After a brief delay of 0.7 μs, the signal indicating the absence of the test signal goes high. This signal increases the counter in the detection system.

![Figure 8](image8.png)  
**Figure 8.** Superposition of physiological signal (simulated as 1 kHz sinusoidal signal) and test signal at amplifier input ($V_{in}$, top). Amplified and filtered test signal ($V_{test}$, center) and physiological signal at filter output ($V_{physio}$, bottom).

![Figure 9](image9.png)  
**Figure 9.** More detailed schematic diagram of the system front-end of Fig. 2 used for simulation. Split transistors in the OTA input and switch are included to simulate a GOS.

![Figure 10](image10.png)  
**Figure 10.** Output of the test signal filter and the digital alarm signal before the counter. The test signal disappears after a GOS is simulated at $t = 10$ μs. The counter receives the signal to count up with a 0.7 μs delay.

4. Results

The system was fabricated in 0.35-μm CMOS integrated circuit technology. The high-pass and low-pass filter circuits were realized on-chip using conventional CMOS circuits. A test signal generator was also included on the test chip. The test signal amplitude was measured as 1 Vpp. Measurements were performed on a randomly selected chip. The measured gain of the amplifier was 170 V/V with a cut-off frequency of 31 kHz. The measured gain at 1 MHz was 5 V/V. The bandwidth was thus smaller than the simulated value, resulting in a reduced high-frequency gain. The reduced bandwidth is explained by the additional load capacitance of the measurement probe. Figure 11 shows an oscilloscope screenshot which shows the drive voltage for the defect-emulating switch (signal defect in Fig. 9) on channel 2. The amplifier output voltage is shown on channel 1. It is observed that the amplifier output settles towards the negative supply voltage after the defect switch is activated. The test signal is visible before the defect and disappears immediately following the defect activation.

![Figure 11](image11.png)  
**Figure 11.** CH1 shows the test signal at the output of the amplifier. CH2 shows the control voltage for the defect-emulating switch.

Figure 12 shows the response of the alarm circuit output on channel 2. Channel 1 shows the output of the high-pass filter ($V_{test}$). The time delay between the disappearance of the test
signal oscillation and the raising of the alarm output was measured as 7.7 μs. This corresponds to 7 full clock cycles of the alarm counter. Thus, the defect condition was detected by signal \( V_{\text{count}} \) less than 700 ns after the defect occurred.

![Figure 12](image-url) Test signal at the high-pass filter output on CH1. It disappears after the GOS switch is activated. This condition is signaled by the alarm circuit after 7.7 μs. Different from Fig. 10, this signal is observed after the counter, resulting in the intended longer delay.

To examine the system performance in a practical application, the test chip was used to acquire an ECG. The ECG was chosen as an example because it does not require dedicated transducers and is well defined. Three disposable gel electrodes were directly connected to the amplifier input and the third electrode was connected to the chip analog ground. The authors thank the National Science Council of Taiwan for supporting this work under grant NSC 99-2221-E-110-023 and the Chip Implementation Center (CIC) for providing integrated circuit manufacturing.

![Figure 13](image-url) Output of the low-pass filter when the circuit is used for ECG detection.

### Table 1. System specification of the test chip (measured).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifier gain</td>
<td>44 dB</td>
</tr>
<tr>
<td>Amplifier cut-off (40 pF load)</td>
<td>31 kHz</td>
</tr>
<tr>
<td>Amplifier cut-off (unloaded)</td>
<td>500 kHz</td>
</tr>
<tr>
<td>Test signal amplitude</td>
<td>1 ( V_{pp} )</td>
</tr>
<tr>
<td>Low-pass filter cut-off</td>
<td>350 kHz</td>
</tr>
<tr>
<td>High-pass filter cut-off</td>
<td>250 kHz</td>
</tr>
<tr>
<td>Alarm hold-off time</td>
<td>7 clock cycles</td>
</tr>
</tbody>
</table>

### 5. Conclusion

A failure monitoring strategy for increased safety in physiological signal recorders which allows the elimination of safety blocking capacitors in patient leads was proposed. The scheme is based on adding a test signal to the physiological input, amplifying the superposed signal, and separating it at the amplifier output. Failure of the amplifier input devices is thus detected. The coupling circuit was analyzed and a test signal output amplitude of around 40 mV at a frequency of 1 MHz was shown to result from a practical choice of parameters. Mismatch analysis showed that the proposed signal coupling scheme tolerates practical parameter variations. An integrated circuit implementation was used to evaluate performance. A GOS in the input stage was emulated. The measurement results confirm that such an event is detectable using the proposed approach. Potential electrical shock due to circuit failure of the input stage can thus be prevented.

### Acknowledgments

The authors thank the National Science Council of Taiwan for providing this work under grant NSC 99-2221-E-110-023 and the Chip Implementation Center (CIC) for providing integrated circuit manufacturing.

### References


